



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,372	12/29/2000	Anthony X. Jarvis	00-BN-051 (STMI01-00051)	8275
30425	7590	11/19/2009	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			LI, AIMEE J	
		ART UNIT	PAPER NUMBER	
				2183
			NOTIFICATION DATE	DELIVERY MODE
			11/19/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

angie.rodriguez@st.com
ip.us@st.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANTHONY X. JARVIS and PAOLO FARABOSCHI

Appeal 2008-006162
Application 09/751,372
Technology Center 2100

Decided: November 17, 2009

Before LEE E. BARRETT, LANCE LEONARD BARRY, and JAMES R. HUGHES, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

The Patent Examiner rejected claims 1-29. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

INVENTION

The invention at issue on appeal is "a data processor capable of executing load operations having different latencies." (Spec. 3.)

ILLUSTRATIVE CLAIM

27. A method, comprising:

shifting, sign extending, or zero extending a first data value from a cache and providing a modified first data value to a first of a plurality of registers; and

transferring a second data value from the cache to a second of the plurality of registers without shifting, sign extending, or zero extending the second data value.

PRIOR ART

Hannah	US 5,706,481	Jan. 6, 1998
Greenley	US 5,761,469	Jun. 2, 1998

REJECTION

Claims 1-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Greenley and Hannah.

ISSUE

The Examiner admits that "Greenley has not explicitly taught bypass circuitry . . . capable of transferring said . . . data value from said data cache directly to said target register without processing said . . . data value in said shifter circuit." (Answer 4.) She concludes, however, that "it would have been obvious to a person of ordinary skill in the art at the time was made to

incorporate the bypassing of Hannah in the device of Greenley to improve system performance." (*Id.* 5.) The Appellants argue that "Greenley, in fact, teaches away from the Examiner's proposed combination and further modification . . ." (App. Br. 24.) Therefore, the issue before us is whether the Appellants have shown error in the Examiner's proposed combination of teachings from Greenley and Hannah.

LAW

"What the prior art teaches and whether it teaches toward or away from the claimed invention . . . is a determination of fact." *Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1088 (Fed. Cir. 1995). "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

FINDINGS OF FACT (FFs)

1. "Referring to FIG. 2 [of Greenley], a detailed block diagram of the alignment unit 170 and the sign extension unit 160 coupled between the data cache 180 and a target register in the register file 150 is shown." (Col. 2, ll. 31-34.)
2. "Since needed data may not be physically stored consecutively in data cache 180, a LOAD access to data cache 180 *must* insure that the accessed data is aligned (i.e. both the upper and lower half of a word is

fetched) into an appropriate format to write into a register in the register file 150." (*Id.* ll. 19-24 (emphasis added).)

3. The same reference includes the following additional description of the alignment unit.

The purpose of the alignment unit 170 is to right justify the data fetched from the data cache 180. For example, when a byte is fetched from the data cache 180, regardless of its byte position (i.e., 0 through 7) in the cache, the byte is *always* right justified in the alignment unit. Similarly, a half word is also right justified in the alignment unit 170, regardless of what position the half word occupied in the cache 180, or even if the two bytes of the half word were present in two different cache lines in the data cache 180. Words, double words, and extended words are similarly aligned by the alignment unit 170. In an unsigned load operation, the rest of the register not loaded with actual data is zero filled.

(*Id.* ll. 34-37 (emphasis added).)

4. "The purpose of the sign extension unit 160 is to fill in the unoccupied bits of a register with sign information indicative of the sign of the data loaded from the data cache 180." (*Id.* ll. 48-50.)

Greenley includes the following additional description of the sign extension unit.

With a byte, the first seven bits (0-6) are used for storing data, the eighth bit (7) stores the sign of the data, and the remaining bits (8-63) are filled with either "0s" or "1s", depending on the sign of the eighth bit. Half-words, words, double-words are similarly sign extended, in the sign extension unit 160.

(*Id.* ll. 56-61.)

ANALYSIS

Greenley interposes an alignment unit 170 and a sign extension unit 160 between a data cache 180 and a target register in a register file 150. (FF 1.) The Examiner finds that the alignment unit and sign extension unit perform the claimed functions of shifting, sign extending, and zero extending a data value from a cache and providing a modified data value to registers. (Answer 16.)

We agree with the Appellants, however, that "Greenley . . . teaches away from the Examiner's proposed combination and further modification by teaching that the shift functions must be used for any data transfer." (App. Br. 24.) More specifically, the reference explains that it *must* insure that data accessed from the cache are aligned into an appropriate format to write into the register file. (FF 2.) Data alignment are *always* performed on bytes and similarly performed on half words, words, double words, or extended words. (FF 3.) Similarly sign extension is performed on accessed data *regardless* of whether the data are bytes, half words, words, or double words. (FF 4.) We find that Greenley's requirement of performing data alignment and sign extension would have discouraged a person of ordinary skill from bypassing the reference's alignment unit and sign extension unit.

CONCLUSION

Based on the aforementioned facts and analysis, we conclude that the Appellants have shown error in the Examiner's proposed combination of teachings from Greenley and Hannah.

Appeal 2008-006162
Application 09/751,372

DECISION

We reverse the rejection of claims 1-29.

REVERSED

rwk

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006